Abstracts

40-Gbit/s D-type flip-flop and multiplexer circuits using InP HEMT (2001 [RFIC])

T. Suzuki, H. Kano, Y. Nakasha, T. Takahashi, K. Imanishi, H. Ohnishi and Y. Watanabe. "40-Gbit/s D-type flip-flop and multiplexer circuits using InP HEMT (2001 [RFIC])." 2001 Radio Frequency Integrated Circuits (RFIC) Symposium 01. (2001 [RFIC]): 291-294.

We developed a novel design technique for a D-type flip-flop (D- FF) circuit that is based on a small-signal-equivalent circuit approach. This technique provides the best condition to operate the D-FF at a high frequency. Using this technique, we fabricated a master-slave D-FF using a 0.15-/spl mu/m InP HEMT technology. We achieved 40-Gbit/s operation with clear-eye-waveform patterns and reduced jitter.

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